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L1 and (determin\$3 same (imbalance or congestion))	23

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<u>L2</u>	L1 and (determin\$3 same (imbalance or congestion))	23	<u>L2</u>
<u>L1</u>	monitor\$3 same activity same bus	2286	<u>L1</u>

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Search Results -

Terms	Documents
L3 and (determin\$3 same (imbalance or congestion))	1

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L4 L3 and (determin\$3 same (imbalance or congestion))

1 L4

L3 monitor\$3 same activity same bus

181 L3

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L2 L1 and (determin\$3 same (imbalance or congestion))

23 L2

L1 monitor\$3 same activity same bus

2286 L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2 and (monitor\$3 same activity)	2

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DB=USPT; PLUR=YES; OP=OR

<u>L4</u>	L2 and (monitor\$3 same activity)	2	<u>L4</u>
<u>L3</u>	L2 and (monitor\$3 near5 activity)	0	<u>L3</u>
<u>L2</u>	5253248.uref.	105	<u>L2</u>
<u>L1</u>	5253248.pn. or 5799161.pn. or 5838931.pn.	3	<u>L1</u>

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» Key

IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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Hardware evaluation of low power communication mechanisms for transport-triggered architectures

Pionteck, T. Garcia, A. Kabulepa, L.D. Glesner, M.
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This paper appears in: Rapid Systems Prototyping, 2003. Proceedings. 14th IEEE International Workshop on

Publication Date: 9-11 June 2003

On page(s): 141 - 147

Number of Pages: xii+242

ISSN: 1074-6005

INSPEC Accession Number: 7816888

Posted online: 2003-06-25 15:31:20.0

Abstract

The requirement for flexibility in IP-based designs increases the attractiveness of transport-triggered architectures as a suitable alternative to classic operation-triggered processors. Since the performance of these architectures strongly depends on the communication mechanism, the optimization of the bus structure represents a major design concern. In this work, a rapid prototyping methodology is employed in order to compare the power consumption and hardware requirements of several competing communication alternatives. Therefore, a generic test processor has been prototyped onto an FPGA. By monitoring the switching activity and bus statistics under realistic operation conditions, a fast and accurate evaluation of different bus coding schemes has been achieved.

Index Terms

Inspec

Controlled Indexing

computer architecture field programmable gate arrays performance evaluation system buses

Non-controlled Indexing

FPGA IP-based design architecture performance bus coding bus statistics bus structure optimization field programmable gate array flexibility requirement generic test processor prototype hardware evaluation hardware requirement low power communication mechanism operation-triggered processor power consumption processor design rapid prototyping methodology switching activity monitoring transport-triggered architecture

Author Keywords